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REMARKS

At the outset, the Examiner is thanked for the thorough consideration given the subject application. Claims 1-27 are currently pending in this application, with claims 1, 9, and 17 amended and claims 25-27 new added. Reconsideration and reexamination are respectfully requested.

The Examiner rejected claims 1-24 under 35 USC § 103(a) as being unpatentable over Applicants' Figures 1-6 in view of Nakahara et al. (US Pat. No. 5,982,470); and rejected claims 1-24 under 35 USC 103(a) as being unpatentable over Applicants' Figures 1-6 in view of Hayakawa et al. (US Pat. No. 6,172,732). Applicants respectfully traverse this rejection.

Claim 1 now recites an element "wherein the gate dummy patterns are formed into the same vertical structure as any one of the gate links and the data links." This allows the dummy patterns to be formed in the same manner as the gate and data links resulting in easier fabrication of the dummy links. Further, claim 1 recites a combination of elements including "a semiconductor layer on the gate insulating film." The insulating film is on the gate link, which includes gate dummy patterns, so the gate dummy patterns include a semiconductor layer. The semiconductor layer has the benefit of preventing a short or electrical mutual action between the gate metal layers and the data metal layers. None of the cited references, singly or in combination, teaches or suggests at least these features of the invention.

The Examiner admits that Applicants' Figures 1-6 do not disclose gate dummy patterns. The Examiner cites Nakahara et al. and Hayakawa et al. in an attempt to cure the deficiencies of Applicants' Figures 1-6.

Nakahara et al. teaches connection terminals 18 placed at high density so as to correspond to TAB (Tape Automated Bonding), etc., on the side of the external circuit. "[T]he sinuous electrode sinuates from the scanning electrode towards the connection terminal 18."

Column 8, lines 5-11. "[A]n electrode having the same thickness as the sinuous electrode 19 is formed as a dummy electrode in order to achieve a uniform thickness of the seal 5." Column 8, lines 32-41. "[B]etween-electrode dummy electrodes 47 are formed along a space between the sinuous electrodes 23 formed on the substrate 1." Column 33, lines 4-9. Nakahara et al. fails to teach gate dummy patterns with a semiconductor layer or gate dummy patterns with the same vertical structure as any one of the gate links and the data links.

Like Nakahara et al., Hayakawa et al. teaches "[d]isposed on one electrode substrate which includes one insulating substrate made of transparent glass which constitutes part of the liquid crystal display device, are display electrodes 46-1 to 46-10 which are made of transparent conductive film and wired in parallel to constitute pixels, terminal electrodes (connection electrodes, i.e., input electrodes) 41-1 to 41-10 connected to the electrodes (output outer lead) of the TCP...." Column 6, lines 8-18. "[D]ummy electrodes 43 provided in the spaces between the terminal electrodes 41-n within the area of the sealing material 44 of the liquid crystal display device and within the so-called frame portion which is a non-lighting portion outside the display portion (the lighting portion) in which the electrodes of the upper and lower electrode substrates intersect." Column 9, lines 19-36. Hayakawa et al. fails to teach gate dummy patterns with a semiconductor layer or gate dummy patterns with the same vertical structure as any one of the gate links and the data links.

Nakahara et al. and Hayakawa et al. may teach dummy electrodes, but the references fail to teach explicitly or implicitly, gate links having gate dummy patterns as in claims 1, 9, and 17. Nakahara et al. and Hayakawa et al. do not teach or suggest the claimed invention as a whole. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983); see also *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976).

Applicants submit that the Examiner has failed to establish a prima facie case of obviousness. Applicants respectfully request that the rejection under 35 USC 103(a) be withdrawn.

Moreover, claims 2-8, 10-16, and 18-24, as well as new claims 25-27, are allowable by virtue of their dependence on claims 1, 9, and 17, which are believed to be allowable.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Dated: April 29, 2003

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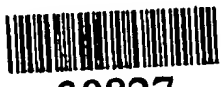

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A liquid crystal display device comprising: a gate electrode, a gate pad and gate links on a substrate, the gate links having gate dumpy patterns;

a gate insulating film on the gate electrode and the gate link;

a semiconductor layer on the gate insulating film;

a source electrode, a drain electrode, a data pad and data links on the semiconductor layer;

a protective film on the source and drain electrodes and the data link; and

a pixel electrode on the protective film,

wherein the gate dummy patterns are formed into the same vertical structure as any one of the gate links and the data links.

9. (Amended) A method of fabricating a liquid crystal display device, comprising:

forming a gate electrode, a gate pad and gate links on a substrate, the gate links having gate dummy patterns;

forming a gate insulating film on the gate electrode and the gate link;

forming a semiconductor layer on the gate insulating film;

forming a source electrode, a drain electrode, a data pad and data links on the semiconductor layer;

forming a protective film on the source and drain electrodes and the data link; and forming a pixel electrode on the protective film,

wherein the gate dummy patterns are formed into the same vertical structure as any one of the gate links and the data links.

17. (Amended) A method of fabricating a liquid crystal display device, comprising:

forming a gate electrode, a gate pad and gate links on a substrate, the gate links having gate dummy patterns;

forming a gate insulating film a semiconductor layer on the gate electrode and the gate link;

forming a source electrode, a drain electrode, a data pad and data links on the

semiconductor layer;

forming a protective film on the source and drain electrodes and the data link; [and]

patterning the gate insulating film, the semiconductor layer, and the protective film, and

forming a pixel electrode on the protective film,

wherein the gate dummy patterns are formed into the same vertical structure as any one of the gate links and the data links.